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### 51. With contact to **source** or **drain** region of refractory material (e.g., polysilicon, tungsten, or silicide) - Patent ...

... to have a stripe-like **shape** and with a ... reductions in **current** density, in turn, reduce the **source-to-drain** turn on ... Efficient **source/drain** interface, MOS transistor and standard ...

With\_contact\_to\_source\_or\_drain\_region... - 48k - [Cached](#) - [More from this site](#) - [Save](#)

### 52. Chapter 4 Modeling of the Enclosed Layout Transistor (PDF)

... **Drain and Source diffusion**. A. Figure 4.1: ELT **shape**. The transistor ... with the **drain current** of standard devices with ... output conductance in an MOS transistor right in the center. The dotted ...

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### 53. Experiment 4 - MOS Device Characterization

Experiment 4 - MOS Device Characterization. W.T. Yeung and R.T. Howe. UC Berkeley EE 105. 1.0 Objective. In this experiment, you will find the device parameters for an n-channel MOSFET. ... as follows: (**drain** = PIN3 gate = PIN4 **source** = PIN 5 ... If the width of **diffusion** area is 46.5 m ... the MOS enters into the saturation region, the **drain current** should remain ...

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### 54. Microsoft Word - Vol.3 Table of Contents (PDF)

... Equation for Simulating **Diffusion** in Submicron Device Structures 24 ... Approach to Deriving the DC **Drain-Current** Relationships in ... **Source/Drain** junctions to suppress punchthrough in ...

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### 55. U.S. Patent: 6025620 - Semiconductor device and method of producing the same - February 15, 2000

... **current** in the junction such as a field edge is large. Therefore, although there was a merit that resistances of the **diffusion** ... of **source/drain** regions in said MOS transistor ...

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### 56. Cours en ligne - CMOS Design - MOS Modeling

CMOS Design > MOS Modeling. MOS Model 3. The MOS model 3 is slightly more complicated than model 1. We show here some of the most important equations. ... **Drain Diffusion**. The lateral **drain diffusion** (LDD) via a ... **current** is the standby **current** appearing between **drain** and **source** for **V<sub>gs</sub>=0** ...

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58. [Quiz answers](#)  
... the area including **source diffusion**, **drain diffusion** and poly gate ... pull-up stack whose **shape** factors are  $3 * 1.2 * 10$  ... a function of programming **current** more than any other parameter ...  
www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/Quiz/qzans.htm - 18k - [Cached](#) - [More from this site](#) - [Save](#)
59. [Lab 1. MOS Device Characterization](#)  
ECE-E432 Microelectronics II. Drexel University Electrical & Computer Engineering. Lab 1. - **MOS Device Characterization**. Written by W.T. Yeung and R.T. Howe for UC Berkeley course EE 105. Modified by K. ... as follows: **drain** = PIN 3, **gate** = PIN 4, **source** = PIN 5 ...  
Comment on the **shape** of the graph ... the **MOS** enters into the saturation region, the **drain current** should remain ...  
www.ece.drexel.edu/courses/ECE-E432/Lab1.MOS\_Devices.html - 21k - [Cached](#) - [More from this site](#) - [Save](#)
60. [United States Patent: 4,829,349](#)  
... the **drain current** in a MOSFET is due to thermionic emission from the **source** which ... the height and **shape** of the potential barrier ... of the effective **diffusion** velocity on the ...  
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In order to increase a cell **drive current**, the phase change memory also ... of the phase change cells are separated by shallow **trench isolation (STI)**. ...

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[N-channel metal oxide semiconductor \(NMOS\) driver circuit and ...](#)  
forming a shallow **trench isolation (STI)** and a gate on a substrate, ... 1A is a **layout diagram** of an **NMOS driver** circuit according to the present invention; ...  
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Shallow **trench isolation (STI)** enabled by chemical mechani- ... indicate a significant **drive current** and clock speed benefit. for high-speed **MOS** devices. ...

[www.vsea.com/news.nsf/files/in%20the%20news/](http://www.vsea.com/news.nsf/files/in%20the%20news/)

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Shallow **trench isolation (STI)**, 135, 137-140, 156-157. Shot noise, 141. Signal integrity analysis, 256 ... high-**current NMOS**-triggered SCR. (HINTSCR), 210 ...  
[media.wiley.com/product\\_data/excerpt/07/04714661/0471466107-2.pdf](http://media.wiley.com/product_data/excerpt/07/04714661/0471466107-2.pdf) -

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[5] H. Yamashina and H. Yamada, "An **MOS current** mode logic ... **shaped CVD-SiO<sub>2</sub> isolation** structure and a BPSG-refilled. **trench**," International Electron ...

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retrograde wells and the use of Shallow **Trench Isolation (STI)**. ... the **drive** capability of the **NMOS**. As a result, both the node ...

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[\[PDF\] Chapter 3 The radiation tolerant layout approach](#)

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The most sensitive parts of an **MOS** transistor from the point of view of the ... increase the node capacitance and the transistor **current drive** capability. ...

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Other structural parameters such as thickness of **trench** sidewall oxide, ... The paper discussed **NMOS** predope enhanced off-state leakage **current** related to ...

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With **trench isolation**,  $V_{th}$  falls as  $W$  falls due to prop. greater  $C$  ... **Current** into the **drive gate's** parasitic diodes and gate overlap (bad) ...

[www.stanford.edu/class/ee371/lectures/lect\\_03\\_transistormodels.pdf](http://www.stanford.edu/class/ee371/lectures/lect_03_transistormodels.pdf) - [Similar pages](#)

[The evolution of IBM CMOS DRAM technology](#)

A p-**MOS** DRAM array built in an n-well CMOS technology meets these ... As a result of the cell **layout**, the **isolation trench** etch, which is done next, ...

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### 1 [Noise considerations for mixed-signal RF IC transceivers](#)

 Sayfe Kiaei, David Allstot, Ken Hansen, Nishath K. Verghese  
 January 1998 **Wireless Networks**, Volume 4 Issue 1
**Publisher:** Kluwer Academic Publishers
 Full text available: [pdf\(629.05 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper discusses design trade-offs for mixed-signal radio frequency integrated circuit (RF IC) transceivers for wireless applications in terms of noise, signal power, receiver linearity, and gain. During air wave transmission, the signal is corrupted by channel noise, adjacent interfering users, image signals, and multi-path fading. Furthermore, the receiver corrupts the incoming signal due to RF circuit non-linearity (intermodulation), electronic device noise, and digital switching noi ...

### 2 [Interconnect scaling implications for CAD](#)

Ron Ho, Ken Mai, Hema Kapadia, Mark Horowitz

 November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
**Publisher:** IEEE Press
 Full text available: [pdf\(91.68 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Interconnect scaling to deep submicron processes presents many challenges to today's CAD flows. A recent analysis by Sylvester and Keutzer examined the behavior of average length wires under scaling, and controversially concluded that current CAD tools are adequate for future module-level designs. In our work, we show that average length wire scaling is sensitive to the technology assumptions, although the change in their behavior is small under all reasonable scaling assumptions. H ...

### 3 [Technical reports](#)



SIGACT News Staff

 January 1980 **ACM SIGACT News**, Volume 12 Issue 1
**Publisher:** ACM Press
 Full text available: [pdf\(5.28 MB\)](#) Additional Information: [full citation](#)

### 4 [Preparing for the future](#)



M. Plazzi, W. Carlson, R. Lucas, M. Schweppe, M. Yanilmaz  
July 1989 **ACM SIGGRAPH Computer Graphics , ACM SIGGRAPH 89 Panel**  
**Proceedings SIGGRAPH '89**, Volume 23 Issue 5

**Publisher:** ACM Press

Full text available: [pdf\(8.64 MB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Welcome to Preparing for the Future, a panel on educational issues in computer graphics. The field of computer graphics education, as no other, combines the disciplines of science and art, and in this sense presents computer graphics instructors in both art and science with some unique problems not faced by their counterparts in other fields. As computer graphics courses become a standard addition in art and science curricula, the way in which we prepare students for this evolutionary field is ch ...

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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

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 Bhattacharya, S.; Banerjee, S.K.; Lee, J.C.; Tasch, A.F., Jr.; Chatterjee, A.;  
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 Shiao-Shien Chen; Tung-Yang Chen; Tien-Hao Tang; Jin-Lian Su; Tzer-Min Si

Chen;

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Volume 50, Issue 7, July 2003 Page(s):1683 - 1689

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